

## Integrated Design, Verification and Reuse for FPGA design flows International Seminar

7 July 2010 at 9.00 am

Venue: Technology Park Ljubljana, Slovenia  
[Tehnoloski park 19](#), building B, conference hall

### Seminar Programme

08.30 – 09.00	Registration with morning coffee
09.00 – 10.30	<b>Accelerating RTL Reuse</b>
10.30 – 10.45	Coffee break
10.45 – 12.00	<b>Automatic RTL Code Quality Assessment</b>
12.00 – 13.00	Buffet lunch at Technology Park Ljubljana Atrium
13.00 – 14.30	<b>Requirements Tracking</b>
14.30 – 14.45	Coffee break
14.45 – 16.30	<b>Using Assertion Monitors for automatic functional checks</b>
16.30 – 17.00	<b>Questions &amp; discussion</b>

Detailed program is available on [WEDAsoft official website](#).

The Lecturer: Neil Rattray



Neil Rattray holds a B.Eng in Electronic Engineering from Queen Mary College, University of London, and has over 20 years experience in ASIC and FPGA design. He worked initially for 8 years for several defence companies in the UK. From there, he went into applications engineering for first Actel and then Xilinx distributors where he supported many customers across the UK and Ireland. He then worked for 7 years for Saros Technology supporting numerous EDA vendors, including Mentor. For the past 18 months Neil has worked as an Application Engineer supporting Mentor's line of Functional Verification Projects across Europe.

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**Registration is obligatory** and should be sent to Kaja Rangus by e-mail: [kaja.rangus@tp-lj.si](mailto:kaja.rangus@tp-lj.si).  
Deadline for submitting the application form is **5<sup>th</sup> July 2010**.

Number of participants is strictly limited. Participation is free of charge.